WHAT IS CLAIMED IS:

1. A semiconductor device including a protection circuit protecting a semiconductor integrated circuit from electrostatic discharge,

the protection circuit comprising:

a detection circuit detecting the electrostatic discharge;

a trigger circuit generating a trigger signal based on the output signal of the detection circuit;

a thyristor having a PNP transistor and an NPN transistor, and operating by the trigger signal from the trigger circuit, the PNP transistor having an emitter connected to a first terminal of the semiconductor device, the NPN transistor having an emitter connected to a second terminal of the semiconductor device and a collector connected to base of the PNP transistor; and

a switching element controlling the connected between the PNP and NPN transistors in accordance with the output signal of the detection circuit.

2. The device according to claim 1, wherein the detection circuit is composed of a resistance element and a MOS (Metal Oxide Semiconductor) capacitor connected between the first and second terminals of the semiconductor device, and the output signal is fetched from the intermediate terminal.

3. The device according to claim 1, wherein the

trigger circuit comprises an inverter circuit, which is composed of: a first MOS (Metal Oxide Semiconductor) transistor having a source connected to the first terminal of the semiconductor device; and a second MOS transistor having a source connected to the second terminal of the semiconductor device and a drain connected in common with the first MOS transistor, wherein each gate of the transistors is inputted the output signal from the detection circuit,

the trigger circuit supplying the trigger signal from the commonly connected drain to a base of the NPN transistor.

4. The device according to claim 1, wherein the trigger circuit includes:

a first inverter circuit, which is composed of: a first MOS (Metal Oxide Semiconductor) transistor having a source connected to the first terminal of the semiconductor device; and a second MOS transistor having a source connected to the second terminal of the semiconductor device and a drain connected in common with the first MOS transistor, wherein each gate of the transistors is inputted the output signal from the detection circuit; and

a second inverter circuit, which is composed of: a third MOS transistor having a source connected to the first terminal of the semiconductor device; and a fourth MOS transistor having a source connected to the

second terminal of the semiconductor device and a drain connected in common with the third MOS transistor, wherein each gate of the transistors is inputted with the output signal from the commonly connected drain in the first inverter circuit,

the trigger circuit supplying the trigger signal from the commonly connected drain in the second inverter circuit to a base of the PNP transistor.

5. The device according to claim 1, wherein the trigger circuit includes:

a first inverter circuit, which is composed of: a first MOS (Metal Oxide Semiconductor) transistor having a source connected to the first terminal of the semiconductor device; and a second MOS transistor having a source connected to the second terminal of the semiconductor device and a drain connected in common with the first MOS transistor, wherein each gate of the transistors is inputted the output signal from the detection circuit; and

a second inverter circuit, which is composed of: a third MOS transistor having a source connected to the first terminal of the semiconductor device; and a fourth MOS transistor having a source connected to the second terminal of the semiconductor device and a drain connected in common with the third MOS transistor, wherein each gate of the transistors is inputted with the output signal from the commonly connected drain in

the first inverter circuit,

the trigger circuit supplying the trigger signal from the commonly connected drain in the second inverter circuit to a base of the NPN transistor.

6. The device according to claim 1, wherein the trigger circuit comprises an inverter circuit, which is composed of: a first MOS (Metal Oxide Semiconductor) transistor having a source connected to the first terminal of the semiconductor device; and a second MOS transistor having a source connected to the second terminal of the semiconductor device and a drain connected in common with the first MOS transistor, wherein each gate of the transistors is inputted the output signal from the detection circuit,

the trigger circuit supplying the trigger signal from the commonly connected drain to a base of the PNP transistor.

7. The device according to claim 1, wherein the switching element is a P-channel MOS (Metal Oxide Semiconductor) transistor.

8. The device according to claim 1, wherein the switching element is formed in a well region formed with the PNP transistor via an isolation region.

9. The device according to claim 1, wherein a base length of the PNP transistor is smaller than a distance from the emitter to a well region formed with the NPN transistor, and a base length of the NPN

transistor is smaller than a distance from the emitter to a well region formed with the PNP transistor.

10. The device according to claim 1, wherein the switching element is connected between a collector of the PNP transistor and a base of the NPN transistor.

11. The device according to claim 1, wherein the switching element is in an off state is when operating under normal power supply voltage.

12. The device according to claim 1, wherein the detection circuit is composed of a resistance element and a MOS (Metal Oxide Semiconductor) capacitor,

the switching element is a P-channel MOS (Metal Oxide Semiconductor) transistor, and

a gate of the P-channel MOS transistor is electrically connected to the first terminal via the resistance element.

13. The device according to claim 1, wherein the first terminal is intended to be supplied with power while the second terminal is intended to be grounded.

14. The device according to claim 2, wherein the resistance element is connected between the first terminal and an output signal of the detection circuit, and the MOS capacitor is connected between the second terminal and the output signal of the detection circuit.

15. The device according to claim 1, wherein the switching element is an N-channel MOS (Metal Oxide

Semiconductor) transistor.

16. The device according to claim 2, wherein the MOS capacitor is connected between the first terminal and the output signal of the detection circuit, and the resistance element is connected between the second terminal and the output signal of the detection circuit.

17. A semiconductor device comprising:

a detection circuit connected between first and second terminals;

a trigger circuit connected between the first and second terminals, and generating a trigger signal in accordance with an output signal of the detection circuit;

a thyristor control circuit generating a thyristor control signal in accordance with the output signal of the detection circuit; and

a thyristor connected between the first and second terminals so that the operation can be controlled based on the trigger signal and the thyristor control signal.

18. A semiconductor device comprising:

a semiconductor integrated circuit connected between first and second terminals;

a detection circuit connected between the first and second terminals;

a trigger circuit connected between the first and second terminals, and generating a trigger signal in

accordance with an output signal of the detection circuit;

a thyristor control circuit generating a thyristor control signal in accordance with the output signal of the detection circuit;

a thyristor connected between the first and second terminals so that the operation can be controlled based on the trigger signal and the thyristor control signal; and

a protection diode connected between the first and second terminals.